

CLAIMS

1. A semiconductor element comprising: a first semiconductor region (2) of a first conductive type; a second semiconductor region (3) of a second conductive type which is formed on said first semiconductor region (2); a third semiconductor region (6) of a first conductive type which is formed in a predetermined surface area of said second semiconductor region (3); a fourth semiconductor region (7) of a first conductive type which is formed in a surface area of said third semiconductor region (6) and has a higher impurity concentration than said third semiconductor region (6) has; and a fifth semiconductor region (8) which is formed in a surface area of said second semiconductor region (3) so as to surround said third semiconductor region (6),

wherein:

said third semiconductor region (6) has a central portion (6a) which surrounds said fourth semiconductor region, and a peripheral portion (6b) which surrounds said central portion (6a);

said central portion (6a) is formed to have a depth from a surface of said second semiconductor region (3) that is deeper than that of said peripheral portion (6b); and

said second semiconductor region (3) arranged right under said central portion (6a) has a smaller amount of electric charges than an amount of electric charges of said second semiconductor region (3) arranged right under said peripheral portion (6b), because said second semiconductor region (3) arranged right under said central portion (6a) has a thickness thinner than that of said second semiconductor region (3) arranged right under said peripheral portion (6b).

2. The semiconductor element according to claim 1, further comprising: a drain electrode (12) formed on said fourth semiconductor region (7); a source electrode (13) formed on said fifth semiconductor region (8); a gate insulation film (10) covering said second semiconductor region (3) between said third semiconductor region (6) and said fifth semiconductor region; and a gate electrode (11) formed on said gate insulation film

(10).

3. The semiconductor element according to claim 2, further comprising: an isolation region (4) of a first conductive type which is formed at an outer edge of said second semiconductor region (3); and a sixth semiconductor region (5) which is formed in
5 a surface area of said second semiconductor region (3) so as to contact said isolation region (4), wherein said second semiconductor region (3) which is present right under said sixth semiconductor region (5) has a same thickness as that of said second semiconductor region (3) which is present right under said peripheral portion (6b).

4. The semiconductor element according to claim 3, wherein said third
10 semiconductor region (6) is formed at generally a center of a surface of said second semiconductor region (3), and said fourth semiconductor region (7) is formed at generally a center of a surface of said third semiconductor region (6).

5. The semiconductor element according to claim 4, further comprising a ground electrode (15) which is formed on said isolation region (4), wherein said second
15 semiconductor region (3) and said third semiconductor region (6) are substantially depleted when a voltage of a predetermined level is applied to between said gate electrode (11) and said drain electrode (12) and said ground electrode (15) is grounded.

6. The semiconductor element according to claim 5, wherein:
said second semiconductor region (3) right under said central portion (6a) has such
20 an amount of electric charges as to maintain an electric charge balance near said fourth semiconductor region (7) in a case where a voltage level of a voltage applied to said fourth semiconductor region (7) is a ground level; and

said second semiconductor region (3) right under said peripheral portion (6b) has such an amount of electric charges as to maintain an electric charge balance near said
25 fourth semiconductor region (7) in a case where a voltage level of a voltage applied to said fourth semiconductor region (7) is a high level in a plus direction with respect to the ground level.

7. A manufacturing method of a semiconductor element comprising:

a step of forming a second semiconductor region (3) of a second conductive type on a semiconductor substrate (2) which constitutes a first semiconductor region of a first conductive type;

5 a step of forming in a surface area of said second semiconductor region (3), a third semiconductor region (6) of a first conductive type which includes a central portion (6a) and a peripheral portion (6b) having different depths from each other, wherein said central portion (6a) is formed in a predetermined surface area of said second semiconductor region (3), and said peripheral portion (6b) is formed in a surface area of
10 said second semiconductor region (3) so as to abut on said central portion (6a) and surround said central portion (6a) and to have a depth shallower than the depth of said central portion (6a); and

a step of forming a fourth semiconductor region (7) of a first conductive type having a higher impurity concentration than said third semiconductor region (6) has, in a surface
15 region of said central portion (6a) included in said third semiconductor region (6).